REMARKS

Claims 1-120 are now pending in the application. Claims 35-38, 39-43, 70-73, 74-78, 112-115, 116-120 are allowed. Applicants would like to thank the Examiner for the courtesy extended during the personal interview conducted on March 23, 2006. During the interview, Applicants' representative and the Examiner discussed differences between the invention and the cited art. No agreement was reached. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

CLAIM OBJECTIONS

Claims 2 and 3 stand objected to for certain informalities. In particular, the Examiner notes that claims 2 and 3 include an undefined acronym. Applicants have amended the claims according to the Examiner's suggestions. Therefore, reconsideration and withdrawal of this objection are respectfully requested with no change in scope.

SPECIFICATION

The specification stands objected to for certain informalities. Applicants have amended the specification according to the Examiner's suggestions. Therefore, reconsideration and withdrawal of this objection are respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-5, 11, 13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-93, and 97 are rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Zaidi et al., U.S.

Pat. No. 6,601,126 and Jim Handy (The Cache Memory Book, second edition, published 1998). This rejection is respectfully traversed.

With respect to Claim 1, Zaidi either singly or in combination with Handy, fails to show, teach, or suggest a line cache that receives a second address that is based on the first address and includes a memory select portion, and a switch that receives the second address and that selectively connects said line cache to one of said first and second memory interfaces based on the memory select portion.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, Zaidi fails to disclose the limitation of a switch that receives the second address and that selectively connects said line cache to one of said first and second memory interfaces based on the memory select portion.

An exemplary embodiment of Applicants' invention shown in FIG. 3 illustrates a switch 64 that selectively connects a line cache 58 to one of a buffer memory and a flash memory based on a memory select portion 134 (or 134'). A translated address 130 (or 130') includes the memory select portion 134 (134'). For example, "[w]hen the buffer memory 79 is selected, the translated address 130 includes a memory select portion 134, which selects the buffer memory 79 as the target memory." (Paragraph [0046]). Similarly, "[w]hen the flash memory 86 is selected, the translated address 130' includes a memory select portion 134', which selects the flash memory 86 as the target

memory." (Paragraph [0047]). The switch 64 selectively connects the line cache 58 to the appropriate memory device (i.e. outputs the translated address) based on the memory select portion 134 or 134'.

In contrast, Zaidi does not includes such a structure. The Examiner alleges that Column 23, Lines 41-45 of Zaidi disclose a switch that selectively connects said line cache to one of said first and second memory interfaces. The cited portion of Zaidi states:

> A switched channel memory controller can be configured to allow particular DMAs or CPUs to access only certain channels. For example, a CPU instruction bus can be connected to an external flash memory through one channel, or an external SDRAM memory through another channel.

Applicants respectfully submit that the cited portion refers only to direct memory access (DMAs) and is absent of any teaching or suggestion of cache memory. In other words, the cited portion does not disclose a switch that receives the second address and that selectively connects said line cache to one of said first and second memory interfaces based on the memory select portion.

The Examiner further relies on FIG. 1. For example, FIG. 1 discloses a cache memory 126 that is connected to a bus 130 via a channel 128. The bus 130 is connected to a MAC 140. The MAC 140 communicates with both a flash memory 106 and an SDRAM 108 via a bus 104. The Examiner alleges that the MAC 140 is a switch that selectively connects the cache memory 126 to one of the flash memory 106 and the SDRAM 108. Applicants respectfully disagree. The MAC 140 is not a switch that selectively connects the cache memory 126 to either the flash memory 106 or the SDRAM 108. The MAC 140 is connected to the flash memory 106 and the SRAM 108

via a common bus (the shared memory bus 104). In other words, the MAC 140 does not selectively connect to one of the flash memory 106 and the SDRAM 108 but is instead always connected via the shared memory bus 104. Zaidi is further absent of any teaching or suggestion that the MAC 140 receives a second address that is based on the first address and includes a memory select portion, and selectively connects based on the memory select portion.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 21, 44, 59, 79, and 98 should be allowable for at least similar reasons.

ALLOWABLE SUBJECT MATTER

The Examiner states that claims 12, 16-19, 29, 32-34, 51, 55-58, 64, 67-69, 90, 94-96, 106, and 109-111 would be allowable if rewritten in independent form. Accordingly, Applicants have amended claims 12, 16, 19, 29, 32, 51, 55, 58, 64, 67, 90, 94, 96, 106, and 109 to include the limitations of the base claim and any intervening claims. Therefore, claims 12, 16, 19, 29, 32, 51, 55, 58, 64, 67, 90, 94, 96, 106, and 109 should now be in condition for allowance.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office

Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: April 7, 2006

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